REMARKS

1. Claims 1-15 were originally presented for examination in this application. In the outstanding Office Action, claims 1-4, 6, and 11-15 have been rejected. Claims 5 and 7-10 were subject to restriction and withdrawn from consideration. By the foregoing Amendments, claim 1, 2, 4, 6, 11, 12, 14 have been amended. Claims 5 and 7-10 have been canceled and no claims have been added. Thus, upon entry of this paper, claims 1-4, 6 and 11-15 will be pending in this application. These amendments are believed not to introduce new matter and their entry is respectfully requested.

2. Based upon the above amendments and following remarks, Applicants respectfully request that all outstanding objections and rejections be reconsidered, and that they be withdrawn.

Election/ Restrictions

3. This application was restricted to one of the following inventions under 35 U.S.C. § 121: Group I including claims 1-4, 6 and 11-15, drawn to halting data strobes on a source synchronous link (classified in class 327, subclass 100); and Group II including claims 5, 7-10, drawn to debug data capture systems (classified in class 375, subclass 221). Applicants affirm that on September 3, 2003 Applicants elected without traverse to prosecute the invention of halting data strobes on a source synchronous link, (claims 1-4, 6 and 11-15). Claims 5 and 7-10, which were withdrawn from further consideration by the Examiner, have been canceled by the foregoing amendments.

Objections to the Specification

4. The Examiner objected to the specification due to various informalities. The specification has been amended in accordance with the Examiner's suggestions, as well as to correct other informalities identified by Applicants. These amendments add no new matter and accommodate the objections to the specification. Accordingly, Applicants respectfully request that the objections to the claims be withdrawn.

Objections to the Claims

5. The Examiner objected to the claims due to various informalities. The claims have been amended in accordance with the Examiner's suggestions thereby

accommodating these objections. Applicants therefore request that the objection to the claims be withdrawn.

Claim Rejections under 35 U.S.C. § 102

4. Claims 1-2 and 11 have been rejection under 35 U.S.C. §102(b) as being anticipated by National Semiconductor DS26C31T/DS26C31M CMOS Quad TRI-STATE Differential Line Driver (hereinafter "National"). Specifically, the Examiner asserts that National discloses a source synchronous link comprising a communication link in a source synchronous receiver and transmitter coupled to the communication link. The Examiner further asserts that National discloses the transmission of data signals as well as data strobe logic configured to generate one or more data strobes that may be halted in a logical state in response to an external condition. The Examiner refers Applicants to the logic diagram on page 4 of National, contending that the figure illustrates both data and data strobe transmit logic in the form of four drivers and that the enable pins to those drivers correspond to Applicants' claimed halting of the data strobes in a predetermined logical state. The Examiner further refers to the illustration on page 6 entitled "Two-Wire Balanced System, RS-422," asserting that a source synchronous receiver and transmitter and a source synchronous communication link are illustrated. Applicants respectfully disagree.

5. National is directed to a quad differential line driver for transmitting digital data over balanced lines. Essentially the component is a buffer that translates TTL or CMOS input levels to RS-422 output levels. In contrast to the Examiner's contentions, National does not disclose a device that manages data strobe signals. In fact, National does not receive, buffer or otherwise process or generate data strobe signals. Taking the logic diagram illustrated on page 4, each of the four drivers are used to transmit data, not data strobes. In fact, a careful review of the input and output signals illustrated on page 1 of National will reveal that the device does nothing more than buffer the noted data input levels. This reveals nothing more than the fact that National translates data signal levels, as noted above. Furthermore, in the diagram illustrated on page 6 entitled "Two-Wire Balanced System, RS-422", the signal reveals nothing more than the transmission of one data slice. Accordingly, National neither teaches nor suggests features of Applicants' invention as recited in independent claim 1. For example, National fails to disclose, teach or suggest "data transmission logic configured to manage the transmission of data signals over at least

one data line of said communication link." Nor does National disclose, teach or suggest a "data strobe transmit logic configured to generate one or more data strobe signals over a corresponding one or more clock lines of said communication link, wherein said data strobe transmit logic halt each said one or more data strobe signals in a selective logical state in response to an external condition." None of these features are even remotely discussed or suggested in National. Accordingly, Applicants respectfully requests that the Section 102 rejection of claims 1 based on National be reconsidered and withdrawn.

6. Claim 4 has been rejected under 35 U.S.C. § 102(b) as being anticipated by Texas Instruments CDC111 1-Line to 9-Line Differential LVPECL Clock Driver (hereinafter "Texas Instruments"). By the foregoing amendments, claim 4 has been canceled thereby rendering this rejection moot.

7. Claim 6 and 11-15 have been rejected under 35 U.S.C. § 102(a) as being anticipated by U. S. Patent No. 6,026,051 to Keeth *et al.* (hereinafter "Keeth"). Specifically, the Examiner asserts that Keeth discloses a source synchronous transmitter for transmission of a differential data strobe over a source synchronous link. That toggled between one of two logical states in a normal mode of operation and with the differential data strobe signals held at one of the logical states when operating in data caption debug of operation. The Examiner refers Applicants to Figure 3 of Keeth, contending that the figure shows the differential outputs DCLK0OUT and DCLK0OUT* make the depicted circuit applicable as a transmitter. The Examiner further contends that the input enable signal is used to set the outputs at one logical state for data capture debug mode, referring to column 3, line 45 of Keeth. Finally, the Examiner contends that Keeth further discloses differential data strobe transmit logic, a differential data strobe signal generator and strobe stopping logic as claimed. The Examiner refers Applicants to Figure 3 in associated description of Keeth in support of this contention. Applicants respectfully disagree.

8. Keeth is directed to a differential receiver for a synchronous DRAM commonly known as a SynchLink-type synchronous dynamic random access memory, or SLDRAM. A differential clock received and amplified by the differential amplifiers switches a set of multiplexes to output a differential output clock. The multiplexes can be disabled by an inactive enable signal, which makes Keeth's differential receiver useful when used in connection with the intermittent data clock

found in SLDRAM. (*See*, Keeth, abstract, cols. 1-2.) The differential receiver 34 illustrated in Figure 3 of Keeth is illustrated as a single block, and the delay circuit in Figure 2 of Keeth. As shown in Figure 2, delay circuit 26 receives differential clock signals as input and outputs differential clock signals as well. The way delay circuit 26 is, in turn, depicted as a single block in the SLDRAM 10 illustrated in Figure 1 of Keeth. There, it is shown that a memory controller 12 exchanges differential clock signals with delay circuit 26 of SLDRAM 10. The function and operations of SDRAM 10 and delay circuit 26 shown in Figures 1 and 2 of Keeth are described in detail in the background of the invention section of Keeth found at columns 1 and 2. The delay circuit 26 generates a delayed right data clock DCLKW and a delayed read data clock DCLKR in response to control signals 28 from the control logic 18 and the data clock signals selected by memory controller 12. Apparently, prior art differential receivers 34 did not have a disable feature to facilitate operation with SDLRAM 10. Keeth discloses such a differential receiver 34 as described in Keeth as illustrated in Figure 3.

9. Keeth neither discloses, teaches nor suggests data strobe transmit logic configured to generate as a differential data strobe, comprising a differential data strobe signal generator that determines logical levels of the data strobe signal and inverse data strobe signals. Nor does Keeth disclose, teach or suggest strobe stopping logic that controls a plurality of logic level signals utilized by the claimed signal generator to cause the data strobe and inverse data strobe signals to remain halted in a desired logical state. Keeth's differential receiver 34 receives the differential data clock DCLK0 and DCLK0* provides for capability of enabling or disabling there input in SLDRAM 10. For at least these reasons, Applicants respectfully assert that Applicants' invention as recited in independent claim 6 is neither disclosed nor suggested by Keeth. Accordingly, Applicants respectfully requests that the rejection of claim 6 be reconsidered and withdrawn.

10. Regarding claim 11, Keeth neither discloses, teaches nor suggests a differential data strobe signal generator that determines the shape of a data strobe signal. And, for at least the reasons noted above, Keeth neither teaches nor suggests Applicants' strobe stopping logic as recited in independent claim 11. Accordingly, for at least the reasons noted above, Applicants respectfully assert that claim 11 is

patentable over Keeth. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

11. The dependent claims are patentable for at least the same reasons as those noted above in connection with their respective base claims.

CONCLUSION

12. Applicants respectfully assert that this application is in condition for allowance. A notice to this effect is respectfully requested.

Respectfully submitted,
Karen Lo *et al.*,

Michael G. Verga, Esq.
Registration No. 39,410

Dated: December 12, 2003
Docket: 10002496-1